08/826,820, filed April 8, 1997, now U.S. Pat No. 5,793,696 which is a continuation of application Serial No. 08/784,927, filed January 16, 1997 now U.S. Patent No. 5,724,300, which is a continuation of application Serial No. 08/576,564, filed December 21, 1995 now U.S. Patent No. 5,615,165, which is a continuation of application Serial No. 08/326,281, filed October 20, 1994 now U.S. Patent No. 5,546,351, which is a continuation-in-part of application Serial No. 07/992,653, filed December 18, 1992 now U.S. Patent No. 5,361,227. --

Page 3, line 23, delete "110"" and insert --"0"--;

Page 11, line 35, delete "B-B'" and insert -- 93-93 --.

line 37, delete "C-C'" and insert -- 94-94 --.

Page 13, line 6, after "a" insert --plurality of memory cells or NAND cells. In the following, one NAND cell will be described.--

line 7, delete "In the".

Page 58, line 15, delete "and (b)" and insert --, (b) and (c) --.

Page 60, line 13, after "problem," insert --as shown in Figure 79--.

Page 71, line 22, delete "B-B" and insert --93-93--;

line 23, delete "C-C'" and insert -- 94-94 --.

IN THE CLAIMS:

Please cancel claims 1-27 without prejudice or disclaimer to the subject matter therein. Please add the following claims:

28. A flash memory system comprising:

a memory unit, including a plurality of flash memory cells, for storing data which can be electrically changed;

wherein said flash memory system

(1) reads out the data stored in said memory unit,

(2) controls said memory unit in order to change the data stored in said memory unit,

(3) detects whether an error has been occurred in read-out data,

(4) corrects errors in the read-out data,